Abstract of the Disclosure

In a synchronous memory device, erroneous operation due to the ripple of the DQS signal in the write operation can be prevented. A synchronous memory device receiving a number of data in synchronous with a rising edge and a falling edge of a clock includes a data strobe buffering unit, a data align latching unit and a DQS signal controlling unit. The data strobe buffering unit outputs a rising pulse and a falling pulse for detecting a rising edge and a falling edge of a DQS signal that sustains high impedance state when there is no operation and is clocked while the data is inputted. The data align latching unit latches and aligns the data in synchronous with the rising pulse and the falling pulse. The DQS signal controlling unit controls the data strobe buffering unit to output the rising pulse and the falling pulse to the data align latching unit only when the DQS signal is clocked.